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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/821,412
Filing Date: April 09, 2004
Appellant(s): LANDIN ET AL.

Stephen J. Curran
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/27/08 appealing from the Office action mailed 12/26/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,434,993	Liencres	7-1995
6,970,872	Chandrasekaran	11-2005
6,065,092	Roy	5-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 – 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Liencres*** (US 5,434,993) in view of ***Chandrasekaran*** (US 6,970,872) and ***Roy*** (US 6,065,092).

In regards to claim 1, Liencres teaches a node ***(see element 20)*** including an active device ***(see element 21)***, an interface to an inter-node network ***(see element 31)***, a memory ***(see element 37)***, and an address network coupling the active device, the interface, and the memory **(see element 33)**; an additional node coupled to the node by the inter-node network ***(see figure 3a; see column 6, lines 11 – 15)***.

In regards to claim 14, Liencres teaches a plurality of devices including a system memory ***(see element 37)***, an active device ***(see element 21)***, and an interface configured to send and receive coherency messages on an inter-node network coupling nodes in the multi-node computer system ***(see element 31)***; an address network configured to convey address packets between the plurality of devices ***(see element 33)***.

In regards to claim 26, Liencres teaches an active device in the node initiating a transaction to gain an access right to a coherency unit by sending an address packet on an address network within the node ***(see element 21)***; an interface in the node ignoring the address packet ***(see element 35)***.

In regard to claims 1, 14, & 26, Liencres does not teach wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the system memory is configured to send a report corresponding to the address packet to the interface if the transaction cannot be satisfied within the node. Liencres teaches ignoring the address packet ***(col. 7, lines 39 – 44)***, but does not teach in response to the report, the interface sending a coherency message to an additional interface in the additional node via

the inter-node network, wherein the coherency message requests the access right to the coherency unit.

However, Chandrasekaran teaches a multi-node network ***(figure 1)*** that employs several techniques to reduce latency. One of the methods employed is "write-time" validity checking ***(col. 6, lines 25 – 36)***. When another node writes out data, it sends out a report stating the latest write time for that data. The read data is invalid once its timestamp comes before the latest write time. The node, now having an invalid read data, will ignore the current address packet ***(col. 2, lines 60 – 66)***, and then have to request the updated data from the additional node. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ optimistic reading of data using "write-time" validity checking so that reads could be employed when another node has exclusive access but hasn't yet written the data.

Also in regard to claims 1, 14, & 26 Liencres does not teach wherein the node has a data network that is separate from the address network. However, it is well known in the art to have separate data and address networks, as cited in Roy ***(col. 3, lines 61 – 67 through col. 4, lines 1 – 5)***. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Liencres's invention by separating the network into separate address and data networks in order to improve performance using interleaving.

For claims 2, 15, & 27, Liencres teaches the node includes a data network coupling the active device, the interface, and the system memory, and wherein the memory is configured to send the report to the interface in a data packet ***(see element 33)***.

For claims 3, 16, & 28, Liencres teaches the address packet is a read-to-own packet ***(see column 7, "Read Transactions")***, the access right is a write access right **(see column 2, lines 4 – 12; "owning" the data will give your write access)**, and wherein the system memory is configured to send the report corresponding to the read-to-own packet to the interface if a global access state of the coherency unit in the node is any global access state other than a modified global access state ***(see column 7, "Read Transactions")***.

For claims 4, 17, & 29, Liencres teaches wherein the node includes an additional active device ***(see element 35)***, wherein the additional active device is configured to transition a read access right to the coherency unit to an invalid access right upon receipt of the read-to-own packet ***(see column 7, "Read Transactions")***.

For claims 5 & 18, Liencres teaches the address network is configured to convey the read-to-own packet in broadcast mode, wherein the active device is configured to gain an ownership responsibility for the coherency unit upon receipt of the read-to-own packet ***(see column 4, lines 45 – 49)***.

For claim 30, Liencres teaches the address network conveying the read-to-own packet in broadcast mode; and the active device gaining an ownership responsibility for the coherency unit upon receipt of the read-to-own packet ***(see column 4, lines 45 - 49)***.

For claim 6, Liencres teaches an additional interface included in the additional node is configured to receive the coherency message on the inter-node network, wherein the additional interface is configured to send a proxy address packet on an address network included in the additional node in response to the coherency message ***(see column 7, "Read Transactions";***

according to [00189] in the applicant's specification, proxy packets are packets sent by the interface 148; the processor cache controller 35 and the interface 148 are one and the same).

For claim 31, Liencres teaches an additional interface included in the additional node receiving the coherency message on the inter-node network; and the additional interface sending a proxy address packet on an additional address network included in the additional node in response to the coherency message ***(see column 7, "Read Transactions"; according to [00189] in the applicant's specification, proxy packets are packets sent by the interface 148; the processor cache controller 35 and the interface 148 are one and the same)***.

For claims 7 & 19, Liencres teaches wherein in response to sending the coherency message, the interface is configured to receive an additional coherency message on the inter-node network; wherein in response to the additional coherency message, the interface is configured to send data corresponding to the coherency unit to the active device ***(see column 8, lines 56 – 62)***.

For claim 32, Liencres teaches the interface receiving an additional coherency message on the inter-node network, wherein the additional coherency message is responsive to the coherency message; in response to the additional coherency message, the interface sending data corresponding to the coherency unit to the active device ***(see column 8, lines 56 – 62)***.

For claims 8 & 20, Liencres teaches the active device is configured to gain the write access right to the coherency unit upon receipt of the data ***(see column 7, "Write Transaction")***.

For claim 33, Liencres teaches the active device gaining the write access right to the coherency unit upon receipt of the data ***(see column 7, "Write Transaction")***.

For claims 9 & 21, Liencres teaches the interface is further configured to send data corresponding to the coherency unit to the system memory in response to the additional coherency message, wherein in response to the data, the system memory is configured to update the global access state of the coherency unit in the node to the modified global access state ***(see column 7, "Read Transactions"; see column 1, lines 64 – 68 through column 2, lines 1 – 12)***.

For claim 34, Liencres teaches the interface sending data corresponding to the coherency unit to the system memory in response to the additional coherency message; and in response to the data, the system memory updating the global access state of the coherency unit in the node to the modified global access state ***(see column 7, "Read Transactions"; see column 1, lines 64 – 68 through column 2, lines 1 – 12)***.

For claims 10 & 22, Liencres teaches the system memory is configured to send data corresponding to the coherency unit to the active device if the global access state is the modified state and if the system memory has an ownership responsibility for the coherency unit, wherein the active device is configured to gain the write access right upon receipt of the data ***(see column 7, "Read Transactions")***.

For claim 35, Liencres teaches the system memory sending data corresponding to the coherency unit to the active device if the global access state is the modified state and if the system memory has an ownership responsibility for the coherency unit; and the active device gaining the write access right upon receipt of the data ***(see column 7, "Read Transactions")***.

For claims 11 & 23, Liencres teaches the address packet is a read-to-share packet ***(see figure 1a)***, the access right is a read access right ***(see column 7, "Read Transactions")***, and wherein the system memory is configured to send the report corresponding to the read-to-share

packet to the interface if a global access state of the coherency unit in the node is not a modified global access state or a shared global access state ***(see column 2, lines 15 – 29; the 2 nodes can share data as long as it is not modified)***.

For claim 36, Liencres teaches the address packet is a read-to-share packet ***(see figure 1a)***, the access right is a read access right ***(see column 7, "Read Transactions")***, and wherein said sending the report occurs if a global access state of the coherency unit in the node is not a modified global access state or a shared global access state ***(see column 2, lines 15 – 29; the 2 nodes can share data as long as it is not modified)***.

For claims 12 & 24, Liencres teaches the interface is configured to add a record corresponding to the report to an outstanding transaction queue in response to receiving the report ***(see column 9, lines 32 – 47)***; wherein the interface is configured to add a record to the outstanding transaction queue in response to each address packet specifying a coherency unit that is not mapped by the system memory ***(see element 40)***.

For claim 37, Liencres teaches the interface adding a record corresponding to the report to an outstanding transaction queue in response to receiving the report ***(see column 9, lines 32 – 47)***; and the interface adding a record to the outstanding transaction queue in response to each address packet specifying a coherency unit that is not mapped by the system memory ***(see element 40)***.

For claims 13 & 25, Liencres teaches the interface is configured to send a corresponding coherency message on the inter-node network in response to each record in the outstanding transaction queue ***(see element 40; see column 9, lines 32 – 47)***.

For claim 38, Liencres teaches the interface sending a corresponding coherency message on the inter-node network in response to each record in the outstanding transaction queue ***(see element 40; see column 9, lines 32 – 47)***.

(10) Response to Argument

Appellant argues:

> ***Liencres "clearly shows that the memory alluded to ... is a cache memory 37, and not a system memory."***

and

> ***The bus cache controller 31, processor 21, and cache memory 37, are not interconnected as stated in the claim language.***

Examiner response:

The Appellant's disclosure does not draw such a clear picture that the memory in question is strictly a system memory. In section V of the "Summary of Claimed Subject Matter" of the Appeal Brief filed 05/27/08, the Appellant cites element 144A in figure 20 (4th line of the 1st paragraph of page 6) as the system memory. It's important to note that this memory ***is inside of each node*** (elements 140A-140C). The Examiner has cited element 37 as the memory, which is also inside of each node. There is no further definition of a system memory disclosed in the specification, but clearly states that memory 144A can store coherency units as cache lines (page 19, lines 4 – 11). Directory 220A is within memory 144A (figure 2). Further, the cache is

"interconnected" through element 32, from which the memory 37 and the processor 21 are part of so the bus 33 does fit within the claim language.

Appellant argues:

> ***The write time may be kept by a lock manager which returns the write validity information. The data retrieval process in Chandrasekaran can only be started if the data block is available. The data may not be valid but it is still available and the memory system does not have knowledge of the validity.***

Examiner response:

A lock manager is not necessary for Chandrasekaran. The transaction cannot be satisfied if a write time is published after the start of the read, thus invalidating the data. Starting the process is OK, but when the report is published before the read is complete, the transaction cannot be satisfied. The report includes the write time sent out by another node so it is definitely not the requested data.

Appellant argues:

> ***Liencres teaches when a read request cannot be fulfilled, a read request packet is issued which may broadcast a read request.***

Examiner response:

With regard to claims 3, 16, & 28, a read-to-own transaction is used to gain "writable copies of coherency units" (specification page 23, lines 3 - 4 of paragraph [0078]) according to

the application. "Owning" a resource gives the user the ability to write to the data (Liencres, column 2, lines 4 – 12). The "modified access state" is just another way of saying having full write access (specification, line 5 of paragraph [00182]). So having a global access state other than a modified global access state means that another node currently owns the coherency unit and will send its write report after it finishes writing.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,
/Shawn Eland/
Examiner, Art Unit 2188

Conferees:
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Supervisory Patent Examiner, Art Unit 2188
07/06/08

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